COSC 290

Class Exercises #8

* + - 1. How many bits are required to address a 32M x 32 memory if:

1. Main memory is byte addressable?
2. Main memory is word addressable (one word size is 32 bits) ?
3. How many bits are required to address a 16M x 8 memory if:
4. Main memory is byte addressable?
5. Main memory is word addressable (a word size is 8 bits)?
6. Suppose we have four memory modules instead of eight in in Figure 4.6 and 4.7 in text book. Draw the memory modules with the addresses they contain using:
7. high-order interleaving
8. low-order interleaving
9. Suppose that a 16M x 16 main memory is built using 512K x 8 RAM chips and that memory is word addressable.
10. How many RAM chips are necessary?
11. If we were accessing one full word, how many chips would be involved?
12. How many address bits are needed for each RAM chip?
13. How many banks will this memory have?
14. How many address bits are needed for all memory?
15. If high-order interleaving is used, where would address 14 (which is E in hex) be located?
16. If low-order interleaving is used, where would address 14 (which is E in hex) be located?
17. Suppose we have 1G x 16 RAM chips that make up a 32G x 64 memory that uses high-order

interleaving. (This means that each word is 64 bits in size and there are 32G of these words.)

1. How many RAM chips are necessary?
2. Assuming four chips per bank, how many banks are required?
3. How many lines must go to each chip?
4. How many bits are needed for a memory address, assuming it is word addressable?
5. For the bits in part d, draw a diagram indicating many and which bits are used for chip select, and how many and which bits are used for the address on the chip.
6. A digital computer has a memory unit with 32 bits per word. The instruction set consists of 160 different operations. All instructions have an operation cod part(opcode) and two address fields: one for a memory address and one for a register address. This particular system includes sixteen general-purpose, user–addressable registers. Registers may be loaded directly from memory, and memory may be updated directly from the registers. Direct memory-to-memory data movement operations are not supported. Each instruction is stored in one word of memory.
7. How many bits are needed for the opcode?
8. How many hits are needed to specify the register?
9. How many bits are left for the memory address part of the instruction?
10. What is the maximum allowable size for memory in bytes?
11. What is the largest unsigned binary number that can be accommodated in one word of memory?
12. Suppose the RAM for a certain computer has 256M words, where each word is 32 bits long.
13. What is the capacity of this memory expressed in bytes?
14. If this RAM is byte addressable, how many bits must an address contain?
15. If this RAM is word addressable, how many bits much an address contain?